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PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO DATA PROCESSING SYSTEMS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company, of Berlin and Munich, Federal Republic of Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to data processing systems, and in particular to a data processing system comprising peripheral units, including peripheral devices, and a central unit comprising a central processor, a working store, and an automonous input/output unit for data traffic between the central unit and the peripheral devices.

At the present time data processing systems are freqently planned in such a way that they can be freely constructed from individual modules in accordance with the particular requirements of use. Subsequent extensions to the system or the replacement of individual modules should be possible in such a manner that the user can retain a current operational organisation and existing programmes and data. To enable the individual modules of the data processing system to cooperate with one another, they must transmit items of information to one another. These items of information can be items of control information or items of data to be processed by or already processed by the data processing system. The interchange of data between the modules requires that agreements be made concerning the organisation of the traffic and concerning the technical transmission devices. These agreements and the associated technical devices from the so-called interface between two modules. Consequently, the configuration of the modules and the nature of the interfaces between the modules determined the ability of a data processing system to be extended or amended.

In data processing systems in which a plurality of peripheral devices are connected to a central unit (or, considered differently, in data processing systems with a large proportion of input/output operations) the organisation of this data traffic is of major importance. A basic investigation of the possibilities in this respect has been published in "Electronische Rechenanlagen", Ed. 11, (1969), Vol. 3, page 151 to 161, in the article "Organisation des Nachrichtenverkehrs zwischen Zentraleinheiten und peripheren Eihneiten in Datenverarbeitungssystemen". Chapter 5 of this article describes a series of possibilities for data traffic between modules if one module is marked out in relation to all the others. This article also points out the advantages and disadvantages presented by the individual forms of organisation with individual or collective data channels and also by mixed forms. In the case of an individual data channel, transmitters and receivers may be clearly identified and addressed by the channel. In the case of collective data channels either one transmitter and a plurality of receivers, or a plurality of transmitters and only one receiver, can be connected to one channel. In the former case the receiver and in the latter case the transmitter can no longer be clearly determined solely by means of the channel.

As an example of such organisation of the data traffic between a central unit and peripheral devices, Swiss Patent No. 432 063 describes a process and a device for transmitting items of data in a manner which is more detailed and related to practice. The resultant device comprises a central data processing unit with a main store, a micro-programme fixed word store, a calculating unit and a plurality of data and address registers, some of which serve as data input and data output registers for the transmission lines to input/out units. The microprogramme fixed word stored

contains routines for the transmission of items of data and is connected via outputs assigned to these routines to an arrangement of transmission registers. This arrangement serves to control connection paths between the main store, the data and address registers and the calculating unit, and also the data transmission paths to the input/output units. For this purpose it is provided with storage positions which are connected to control signal lines which are common to all the input/output units. Via these control signal lines it is possible to mark the nature of the data on the data transmission paths and control states, relating to these items of data, in the storage positions of the transmission registers.

This known data processing system is therefore a system with collective information channels in relation to the control information. Because, as mentioned above, an input/output unit acting as a transmitter or receiver is no longer clearly determined by the information channel, this known data processing system is operated in such manner that the input/output units are each assigned a control word in a store of the central processing unit, which word contains state data, relating to the relevant input/output unit, of the transmission devices, control data of the relevant transmission operation, and address data for the storage of the items of information or subsidiary information which are to be transmitted. With each data transmission, i.e. even in the case of the transmission of merely a part, the control word is called up for purposes or analysis and up-dating.

Thus in this known data processing system the input/output units, as control units without special data organisation functions, are connected to one or more than one peripheral device. The organisation of the data traffic is assumed by the arrangement of transmission registers which are connected between the input/output units and the main store and which in data processing are frequently referred to as the "channel" which forms part of the central unit.

The above described organisation plan of this known data processing system will show that at any one time only one single input/output unit can be connected to this channel, and therefore an overlapping in time of input and output signals of different input/output units is not possible, and consequently the data transfer rate is limited. In addition, the actual data exchange cannot commence until the transmitting or receiving input/output unit has been marked by the control word. This probably explains why this known data processing system is not very flexible in respect of modifications and extensions with further input/output units, due to the organisation of the data traffic, and also no longer satisfies modern requirements in respect of high data transfer rates.

The aim exists to provide a data processing system which is better suited to development, e.g. extensions, in stages. In addition, in the interests of ecomonical production, it is desirable that processors with similar functions, e.g. input/output units, be similar and at the same time be designed in such manner that they can easily be connected to the system, and a standard operating system should be able to operate arbitrary system configurations to facilitate extensions or modifications of the data processing system.

According to this invention there is provided a data processing system comprising peripheral units, including peripheral devices, and a central unit comprising a central processor, a working store, and an automonous input/output unit for data traffic between the central unit and the peripheral devices, wherein a central control device provides for controlling such data traffic, wherein the input/output unit comprises a plurality of processors connected to form a chain, a first processor in the chain being connected via a standard interface to the central control device and each other processor in the chain being connected via a respective standard interface to the particular preceding processor in the chain, wherein data channels and control signal paths pass via the standard interfaces from the central control device to the processors in the chain, and wherein at least each processor except for the last processor in the chain contains switching means and coordination circuit which is responsive to request and acknowledgement signals, conducted via the control signal paths and produced respectively by the respective processor and by the central control device to select the respective processor for data traffic, to cause the switching means to connect the data channels to the processor and to render such request and acknowledgement signals ineffective in respect of subsequent processor in the chain for the duration of the data traffic over the connected data channels.

The invention enables the data exchange of a central unit of a data processing system with a reasonably priced basic equipment to be adapted, by supplementary modules, to functions involving increased requirements in terms of the number of connection possiblities and/or of data traffic. This basic construction is burdened

as little as possibly by extension possibilities of the system.

The central control device facilitates the connection of up to a predetermined maximum number of processors for a totally developed system, but is independent of the particular stage of development of the system because the coordination circuits are provided in the process or which depending on the system, can be more or less independent processors. At least each processor except for the last processor in the chain feeds the signals of its input interface to the following processors in the chain and coordinates its own requests with those of the following processors.

The outlay for coordination which arises through the interconnection of the processors in proportional to the extent of the development. The connected processors are decoupled from one another so that a guaranteeable reaction time can be given for each processor.

In one embodiment of the invention the control signal paths comprise processor selection control lines and further control lines, the further control lines being conducted via at least each processor except for the last processor in the chain in such manner that the connections of these further control lines to the terminals of the standard interface leading to the subsequent processor in the chain are displaced by one terminal from the connections to terminals of the standard interface leading to the relevant processor, the central control device supplies a first potential to the further control lines connected to it and at least each processor except the last processor in the chain supplies a second, different, potential to that one of said terminals of the standard interface leading to the subsequent processor in the chain which as a result of said connection displacement is otherwise unconnected, and each processor in the chain includes a coding circuit, which serves to form from the signals on the further control lines a binary-coded number assigned to the processor, and a comparator device which compares said binary-coded number with a processor selection number which is transmitted by the central control device over the processor selection control lines in order to select a processor for data traffic, and in the event of identity causes the switching means of the processor to connect the data channels to the processor.

This has the advantage that in dependence upon the position of a processor in the chain, without circuitry alterations, the correct number for the identification of a processor is automatically formed. Thus each processor in the chain has an identical interface and it is solely the nature of the connection of the processors in the chain which determines the formation of the correct number for each processor.

Preferably the switching means in at least each processor except the last processor in the chain includes a switching device which is constituted by AND elements each having a first input connected to the output of the comparator device and a second input connected to a respective one of the lines of the data channel for the transfer of data from the central unit to the peripheral devices, the outputs of the AND elements being connected to an intermediate data store in the processor. Preferably the switching means in at least each processor except the last processor in the chain includes a further switching device which comprises logic elements, each consisting of two AND elements, the outputs of which are linked by a logic OR link, and a further OR element, and in the case of each of said logic elements a respective line of the data channels for the transfer of data from the peripheral devices to the central unit is conducted via a first input of one AND element and the output of the logic OR link towards the central control device, a first input of the other AND element is connected to a respective line connected to a further intermediate data store in the processor, the further OR element having an inverted output connected to a second input of said one AND element and a non-inverted output connected to a second input of said other AND element, the inputs of the further OR element being connected, to the output of the comparator device and to a signal line for requests by the respective processor for the transfer of data.

In an alternative embodiment of the invention the control signal paths comprise selection lines which are conducted via at least each processor except for the last processor in the chain in such manner that the connections of the selection lines to terminals of the standard interface leading to the subsequent processor in the chain are displaced by one terminal from the connections to terminals of the standard interface leading to the relevant processor, and in each such processor it is that selection line which as a result of said connection displacement is not connected to one of the first mentioned terminals which constitutes a signal line for requests for the processor by the central control device.

The invention will be further understood from the following description by way of example of an embodiment thereof with

reference to the accompanying drawings, in which:—

Figure 1 shows a block circuit diagram of a data processing system of modular construction, the system including a central unit having as part of its contents an automonous input/output unit in which as processors a plurality of block multiplexers with independent functions are connected in the form of a chain;

Figure 2 shows a further block circuit diagram illustrating the course of the information channels in such a chain or interconnected processors;

Figure 3 shows the basic details of a coordination circuit which is illustrated in Figure 2 in block form; and

Figure 4 shows a further block circuit diagram of chain-connected processors, illustrating the formation of a processor number in the chain.

The block circuit diagram illustrated in Figure 1 gives a basic illustration of the central unit of modern data processing system of modular construction whose construction and organisation plan, which are known *per se*, are explained in principle below.

The central unit contains an operating store system ASP and a plurality of independently operating units, comprising a central processor ZP, which assumes the actual programme execution by working through the individual commands in user programmes and in the operating system, and an input/output unit EAP, which handles all the input/output operations. The central unit also includes an automonous servicing panel WF, which in itself is not an independent processing unit, which carries out a system and programme control and also carries out fault diagnosis and preventive servicing.

For data traffic between the processor ZP and the unit EAP, the servicing panel WF, and the operating store system ASP, these modules of the central unit are connected via bus lines, indicated in Figure 1 by double lines and arrows, to a coordinator which here is integrated into the input/output unit EAP as a central control device CCU. The bus lines represent line groups which are of similar construction, i.e. possess the same data width and thus also permit identical data rates. Although this is not illustrated in Figure 1, these bus lines are in each case provided in pairs and are always employed only in one transfer direction.

The central control device CCU assumes the organisation of the data traffic via the input/output unit EAP, for which purpose it can be provided with a special micro programme store, and is connected via bus lines to input/output channels. As examples of input/output channels, Figure 1 shows a so-called byte-multiplexer BY-MUX and three block multiplexers BL-MUX1, BL-MUX2 and BL-MUX3. The byte multiplexer BY-MUX permits, via its peripheral terminals or so-called trunks 1 to m, a simultaneous data exchange organised byte-wise. Each of the block multiplexers has only two trunks 0 and 1 to which are connected, for example, peripheral control units PST which are themselves assigned peripheral devices PGE via terminals 1 to n. There the peripheral control units PST carry out the conversion of the standardized control signals supplied by the central unit into signals specifically assigned to peripheral devices. The interfaces between the individual modules up to the input end of a peripheral control unit PST are thus designed as standard interfaces SS, whilst the interface GS between a peripheral control unit PST and a peripheral device PGE is designed to be specifically assigned to the device.

The block multiplexers BL-MUX are similar specialised input/output processors which carry out subsidiary functions in the organisation of the data traffic in automonous fashion and relieve the central control device CCU of load. If a data processing system contains a plurality of similar processors which, apart from their order of priority, enjoy equal rights and which must exchange data and items of control information with the central unit, it is necessary to coordinate this data traffic via the processors. Although this coordination of the data traffic of the block multiplexers BL-MUX could in this case be assigned to the central control device CCU, in a data processing system in which the number of connected processors is dependent upon the stage of development of the system this would be inadvisable, as then in accordance with the stage of development of the system the outlay in the central control device would also have to be increased or alternatively a common, very expensive control device would have to be used for all stages of development and in many cases this would not be employed to full capacity.

An alternative solution to this problem is afforded by this invention and is indicated in Figure 2, in which a series circuit of four processors P1 to P4, which are of similar construction and have similar functions, is represented in a block circuit diagram. The processors P1 to P4 can for example correspond to the block multiplexers BL-MUX shown in Figure 1, but here they have been shown more generally.

The processors P1 to P4 are connected to one another and to the central control device in a chain in each case via a standard

interface SS via which the data channels are conducted for output data AD (i.e. data to be output from the central unit to peripheral devices) and for input data ED (i.e. data to be input to the central unit from peripheral devices) in the reverse direction. The output data AD are available in parallel to each of the processors P1 to P4 via a first switching device S1 in each processor. A second switching device S2 is provided at least in each of the processors P1 to P3 to switch the data channel for input data ED in each processor either to the subsequent processor in the chain or to signal outputs of the respective processor. Thus a processor having a lower ordinal number has priority over subsequent processors in the chain, e.g. the processor P2 has priority over the subsequent processors P3 and P4.

Except for the last of the linked processors, each processor in the chain contains a coordination circuit COR which undertakes the data organisation for itself and the subsequent processors. This is indicated in Figure 2 by broken lines leading from the coordination circuit COR to the switching device S1 and S2 in each of the processors P1 to P3. Paths AS and QS for control signals, (request signals and acknowledgement signals respectively) are conducted via the coordination circuits COR. This illustrates the principle that each coordination circuit COR coordinates the data traffic of its own processor with that of the subsequent processors on the basis of items of control information transmitted in both transfer directions, thus relieving the central control device CCU in the input/output unit of load. It should be noted that in an initial stage of development of the system in which the chain of processes is replaced by only a single processor corresponding to the processor P4 in Figure 2, no such data coordination is necessary. The present invention does not extend to such an initial stage of development of the system but is confined to following stages of development of the system in which at least one further processor having a coordination circuit is connected at the start of the chain i.e. next to the central control device CCU.

As the principle of such processors of an input/output system is already known, in the following description only special features of the coordination circuits COR and standard interfaces SS will be explained.

Referring now to Figure 3, this generally illustrates the series connection in a chain of three processors Pn−1, Pn and Pn+1. The processor Pn−1 shown at the right-hand side of Figure 3 can be constituted by the central control device CCU.

The data channels for output data AD and input data ED are again shown as bus lines. As has been basically already explained with reference to Figure 2, the data channel for output data AD is conducted via the processor Pn and output data intended for this processor are received via the first switching device S1 which is connected to this data channel and are applied to a terminal *a* which has been depicted as a circle. This leads for example to a buffer store or to data registers of the processor in which the output data AD are initially intermediately stored. At a suitable time, they are called up from this point by an internal control of the processor Pn and are transmitted in known manner via input/output lines to peripheral control units and devices. In the first switch device S1 each of the parallel lines of the data channel for output data AD is assigned a respective AND-element, as indicated by the AND-element UG1 shown in Figure 3, via a second input of which the AND element can be enabled in the manner described below.

The data channel for input data ED in the opposite direction is assigned the second switching device S2. This switching device serves to conduct input data ED of processors, such as the processor Pn+1, having lower priorities through the processor Pn, or to switch through input data ED of the processor Pn to the data channel for input data.

As schematically illustrated in Figure 3, the second switching device S2 is provided, for each individual line of the data channel for input data ED, with a logic linking element OG2 in which two AND elements are linked by a logic OR element. One input of one of the two AND elements is connected to a signal line of the data channel for input data ED, which is connected to the adjacent processor Pn+1, and one input of the other of the two AND elements is connected to a signal line of the data channel for input data which leads from the processor Pn. This is indicated in Figure 3 by a line terminal *b* which, similarly to the line terminal *a*, is conducted to a data buffer and to data registers.

The two complementary outputs of an OR element OG1 are connected to second inputs of the two AND elements. As is explained further below, this OR element OG1 is connected so that when the processor Pn is ready to feed input data ED into the data channel the switching device S2 cuts off processors having lower priorities, e.g. the processor Pn+1, from the data channel.

From the transfer of output data AD from the central unit, the central control

device CCU requests a specific processor, e.g. the processor Pn, via first selection lines AW1 which are designed as collective control signal paths. These selection lines AW1 then conduct specific selection signals for the requested processor. Connected to the selection lines AW1 in each processor is a comparator device VE which compares these selection signals with a processor number which is specific to the processor.

This processor number is produced with the aid of further control signal lines PNR in each processor solely on a wiring or line guidance basis. This is shown in more detail in Figure 4, which shows four chain linked processors P1 to P4 connected to one another by three control lines PNR. These control lines PNR are wired in the processors in such manner that the connections to the line terminals of the control signal lines at the output of a processor are laterally displaced from the connections to the line terminals at the input of the processor, in each case in the same direction by one terminal pin. Each terminal pin no longer employed by this wiring for one of the control lines PNR at the output of a processor is connected to earth (potential "Ø").

If it is now provided that all of the control signal lines PNR at the input of the first processor P1 of the chain receive a negative signal potential "L" when the chain is connected up, in each processor a specific signal combination, shown in brackets in Figure 4, is obtained from the control signal lines. This signal combination is specifically assigned to the ordinal number of the processor in the chain and is produced solely as a result of the nature of the wiring of the control signal lines.

As shown in Figure 3, in the processor Pn the input-end terminals of the control signal lines PNR (in this case only two control signal lines PNR are shown) are connected to a coding circuit COD. The coding circuit COD serves to convert or recode the signal combination conducted on the control signal lines PNR into the coding of the selection signals on the selection signal lines AW1. This recoded signal combination represents the processor number and is conducted to the comparator device VE. In the event that the selection signals on the selection signal lines AW1 agree with the recoded signal combination representing the particular processor number, the comparator device VE produces an output signal.

This output signal from the comparator device VE is applied to the two switching devices S1 and S2. When the central control device CCU requests the processor Pn to transfer output data AD, the AND elements of the first switching device S1 are enabled with this output signal so that the output data AD can be transferred into the assigned data buffer of the processor Pn.

In the case of data transfer in the reverse direction, the central control device CCU can likewise emit a request with selection signals via the selection lines AW1. In order to be able to activate the processor Pn for this data transfer, the output of the comparator device VE is connected to one of the two inputs of the OR element OG1 of the second switching device S2. Via the two complementary outputs of this OR element, the two AND elements of the logic linking element OG2 are prepared so that the data channel for input data ED is cut off from the data channel for input data ED of the processor Pn+1 and connected to the data channel assigned to the processor Pn. Items of input data intermediately stored in a data register of the processor Pn are thus able to be transmitted via the terminal *b*.

The processor Pn itself can also request a data transfer for input data ED. For this purpose a control signal line ETAn is connected, via an element IG to the second input of the OR element OG1 of the second switching device S2. This line ETAn receives via a terminal *c* a signal potential in the event of a request from the processor to the central control device CCU for a transfer of input data ED. In the processor Pn this signal has the same effect in controlling the switching device S2 as a request, resulting in an output signal being produced by the comparator device VE, from the central control device CCU to the processor Pn.

In addition such a request for transfer of input data made by the processor must also be communicated as a control signal combination to the central control device CCU. Figure 3 schematically illustrates a further control signal line ETA. This control signal line is conducted, via a further OR element OG3, through the processor Pn. The OR element OG3 can be actuated only with a negative potential, so that an open signal input in the central control device CCU is prevented from simulating a processor request. The element IG produces from a control signal on the control signal line ETAn complementary output signals, the inverted output being connected to the second input of the OR element OG3 and the non-inverted output being connected to the switching device S2 as described above. This control signal for a transfer of input data is produced by an internal control device (not shown) of the processor Pn, which device coordinates the data exchange of the peripheral units connected to the processor with the central unit of the

data processing system in known manner, and as stated above is supplied to the control signal line ETAn via the terminal *c*.

As is shown clearly in Figure 3, the logic signal state of the control signal line ETAn at the input of the inverter element IG is inverted only at that output of the inverter element IG which is connected to the OR element OG3. Thus requests from processors for a transfer of input data ED made to the central control device CCU can be transmitted only with negative potential.

The control signal lines ETA for requests made by processors for transfer of input data have been described above only as one example of a group of control signal lines. All the control signal lines of this group serve to transfer requests from the processors to the central control device CCU and are wired in the same way. Thus the processors can also send to the central control device CCU requests for fault routines, data chains, breaks, etc., with the processor number and other accompanying data. The nature of the request and also the processor number provide specific priorities for these requests in accordance with which the central control device CCU handles and acknowledges these requests.

An example of a control line via which such an acknowledgement signal is emitted is likewise shown in Figure 3. Via an OR-element OG4, similarly to the control signal line ETA but in the reverse direction, a further control signal line SPR is conducted through the processor Pn. This line serves as a blocking signal line by means of which for the duration of data traffic via the processor Pn this processor, via a signal terminal *d* connected to one input of the OR element OG4, prevents lower priority processors from receiving an acknowledgement signal. Via this signal terminal *d*, each processor can feed a blocking signal into the blocking signal line SPR for the subsequent, lower priority, processors in the chain and can thus prevent these lower priority processors from receiving an acknowledgement signal.

Finally, Figure 3 also shows a further possibility of how the central control device CCU can directly select a specific processor. For this purpose further selection lines AW2 are conducted through the processor Pn in such manner that the output of a specific selection line is one terminal pin lower than the input in this illustration. The particular lowest selection signal line without a terminal at the output is connected to an internal terminal *e* of the processor Pn. Therefore a selection signal on a line can only be processed in the processor which is connected internally to this line. This possibility of selecting a processor in the chain in terms of circuitry has the same characteristics as the above described selection carried out via the first selection lines AW1. This is because the manner of wiring of the second selection lines corresponds approximately to that of the control lines PNR for the formation of the processor number. Considered from the central control device CCU, this principle of selection is independent of the stage of development of the data processing system. However, there is a difference in respect of the transit time and the circuitry outlay, between the two selection possibilities.

The second direct selection possibility requires a specific selection line for each chain-linked processor and requires an extra outlay in the central control device CCU, although it has the advantage that selector signals can be directly conducted to a processor without loss of transit time.

It will be appreciated that the above description only relates to basic sequences in a simplified manner. As the construction and the function of input/output controls, like selector channels or multiplex channels, is known *per se*, in the above only special details, relating to the chain linking of processors of an input/output system, the coordination circuit, and the interfaces between the chain connected processors, have been discussed.

In order to clarify the nature of this invention, the drawings have deliberately been schematized, e.g. in the number of illustrated lines. Persons skilled in the art will be aware that, for example, many of the control lines which here have been shown only as single lines in practice can be realised only by a group of lines, as the control signals which here have been explained in simplified fashion as specific groups of signals in each case are constituted by combinations of signals in which specific accompanying signals are contained, for example, serving to safeguard the process sequence. In practice the interface must possess a data width of more than one hundred signals in order to comply with modern data rate requirements in the traffic between a central unit and peripheral units. The above description does not include details of this kind in order to depict clearly the fundamental characteristics in the operation of chain linked processors with individual coordination components. The described circuit details make it clear that with such coordination components it is possible to design the interface between chain linked processors in such manner that these, when of similar construction, serve as arbitrary elements in a chain of processors and can be interconnected

without internal modifications. The operating system of the data processing system treats the chain of processors like a single processor and therefore is independent of the stage of development of the input/output system.

WHAT WE CLAIM IS:—

1. A data processing system comprising peripheral units, including peripheral devices, and a central unit comprising a central processor, a working store, and an automonous input/output unit for data traffic between the central unit and the peripheral devices, wherein a central control device is provided for controlling such data traffic, wherein the input/output unit comprises a plurality of processors connected to form a chain, a first processor in the chain being connected via a standard interface to the central control device and each other processor in the chain being connected via a respective standard interface to the particular preceding process or in the chain, wherein data channels and control signal paths pass via the standard interfaces from the central control device to the processors in the chain, and wherein at least each processor except for the last processor in the chain contains switching means and coordination circuit which is responsive to the request and acknowledgement signals conducted via the control signal paths and produced respectively by the respective processor and by the central control device to select the respective processor for data traffic to cause the switching means to connect the data channels to the processor and to render such request and acknowledgement signals ineffective in respect of subsequent processors in the chain for the duration of the data traffic over the connected data channels.

2. A system as claimed in Claim 1, wherein the control signal paths comprise processor selection control lines and further control lines the further control lines being conducted via at least each processor except for the last processor in the chain in such manner that the connections of these further control lines to terminals of the standard interface leading to the subsequent processor in the chain are displaced by one terminal from the connections to terminals of the standard interface leading to the relevant processor, wherein the central control device supplies a first potential to the further control lines connected to it and at least each processor except the last processor in the chain supplies a second, different, potential to that one of said terminals of the standard interface leading to the subsequent processor in the chain which as a result of said connection displacement is otherwise unconnected, and wherein each processor in the chain includes a coding circuit, which serves to form from the signals on the further control lines a binary-coded number assigned to the processor, and a comparator device which compares said binary-coded number with a processor selection number, which is transmitted by the central control device over the processor selection control lines in order to select a processor for data traffic, and in the event of identity causes the switching means of the processor to connect the data channels to the processor.

3. A system as claimed in Claim 2, wherein the switching means in at least each processor except the last processor in the chain includes a switching device which is constituted by AND elements each having a first input connected to the output of the comparator device and a second input connected to a respective one of the lines of the data channel for the transfer of data from the central unit to the peripheral devices, the outputs of the AND elements being connected to an intermediate data store in the processor.

4. A system as claimed in Claim 2 or Claim 3, wherein the switching means in at least each processor except the last processor in the chain includes a further switching device which comprises logic elements, each consisting of two AND elements, the outputs of which are linked by a logic OR link, and a further OR element, and wherein in the case of each of said logic elements a respective line of the data channels for the transfer of data from the peripheral devices to the central unit is conducted via a first input of one AND element and the output of the logic OR link towards the central control device, a first input of the other AND element is connected to a respective line connected to a further intermediate data store in the processor, the further OR element having an inverted output connected to a second input of said one AND element and a non-inverted output connected to a second input of said other AND element, inputs of the further OR element being connected to the output of the comparator device and to a signal line for requests by the respective processor for the transfer of data.

5. A system as claimed in Claim 1, wherein the control signal paths comprise selection lines which are conducted via at least each processor except for the last processor in the chain in such manner that the connections of the selection lines to terminals of the standard interface leading to the subsequent processor in the chain are displaced by one terminal from the connections to terminals of the standard

interface leading to the relevant processor, and wherein in each such processor it is that selection line which as a result of said connection displacement is not connected to one of the first mentioned terminals which constitutes a signal line for requests for the processor by the central control device.

6. A system as claimed in any of Claims 1 to 5, wherein the control signal paths comprise control lines for requests made by processors to the central control device, wherein at least each processor except the last processor in the chain includes an OR element for each such control line via which the line is conducted in such manner that the processor request are transmitted only with negative potential so that an open signal input in the central control device does not simulate requests, and wherein in each case a signal line for requests of the processor is connected to a second input of the OR element.

7. A system as claimed in any of Claims 1 to 6, wherein the control signal paths comprise additional lines for acknowledgements by the central control device of requests made by processors, wherein at least each processor except the last processor in the chain includes an OR element for each such additional control line via which the line is conducted, and wherein in each case a blocking signal line of the processor is connected to a second input of the OR element whereby the processor can prevent subsequent processors in the chain from receiving acknowledgements from the central control device.

8. A data processing system substantially as herein described with reference to the accompanying drawings.

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1483903 COMPLETE SPECIFICATION
3 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

Fig.1

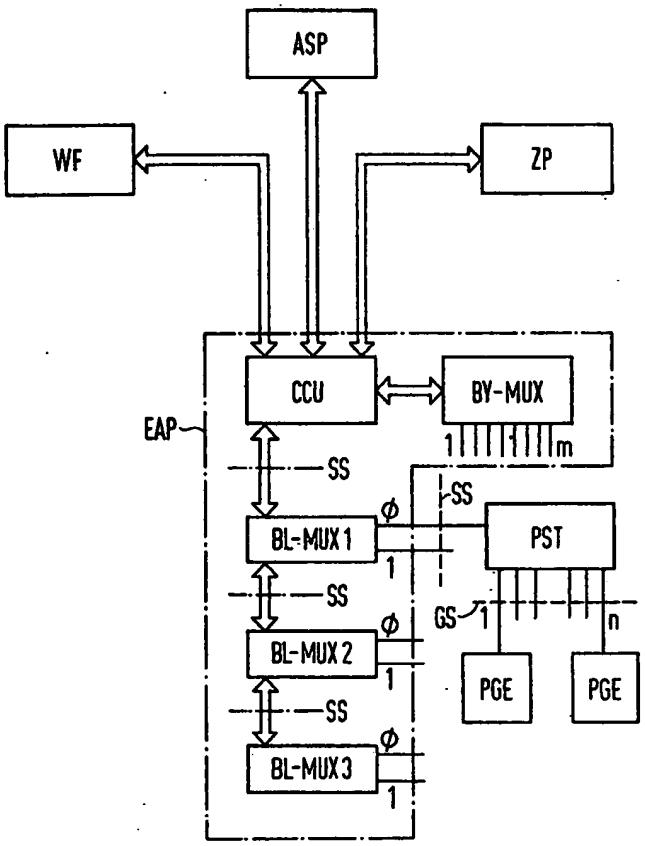
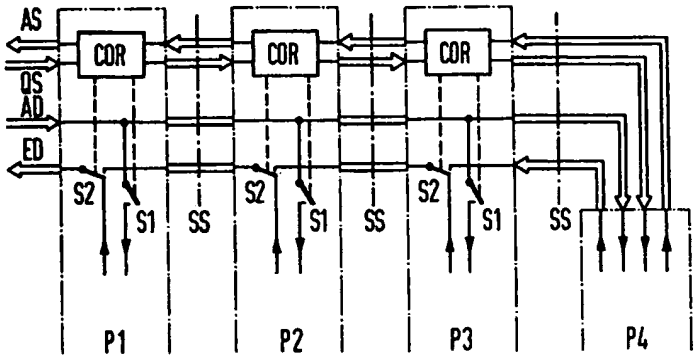


Fig.2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AD
ED
COR
COR
COR
S2
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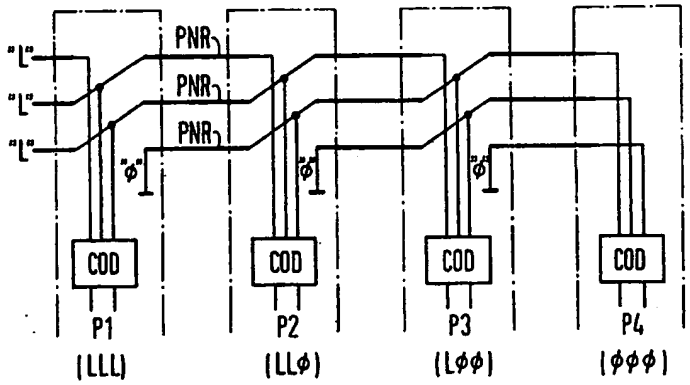
SS
S2
S1
SS
S2
S1
SS
P1
P2
P3
P4

Fig.4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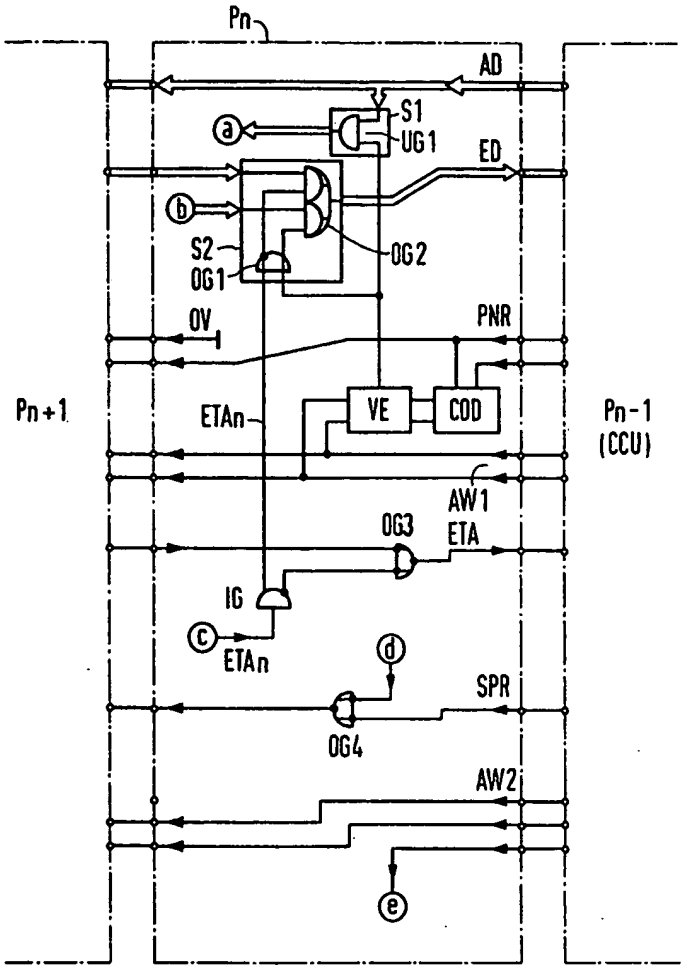
COD
P1
P2
P3
P4
(LLL)
(LLφ)
(Lφφ)
(φφφ)

Fig.3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(CCU)
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ETA
IG
c
ETAn
d
SPR
OG4
AW2
e